L3: Entry 10 of 29 File: USPT Sep 10, 2002

DOCUMENT-IDENTIFIER: US 6449709 B1
TITLE: Fast stack save and restore system and method

Detailed Description Text (4):
The host adapter 140 is an intelligent interface that includes a processor, in the illustrative embodiment called a Multi-Tasking Protocol Engine 250, that controls high-speed data transfer of the interface. The Multi-tasking protocol engine 250 executes protocol commands described by a Transfer Control Block (TCB) and scatter/gather (S/G) lists to control the data transfer between the host system memory and the Fibre Channel connected device.

Detailed Description Text (20):
Each of the send payload buffer 286 and the receive payload buffer 276 data buffer set has a payload manager that contains a Scatter/Gather (S/G) capable Direct Memory Access (DMA) channel for transferring buffer data to/from the PCI local bus 120. The DMA channel contains an S/G element First-In-First-Out (FIFO) buffer (not shown) that allows future S/G list elements to be stored while the current element is being processed by the DMA channel. S/G elements are prefetched from an S/G list cached in a synchronous Static Random Access Memory (SRAM) 142 connected to the Memory Port Interface (MPI) 230 block and stored in the DMA FIFO by the Multi-Tasking Protocol Engine 250. S/G prefetching to the DMA FIFO minimizes the transfer delay to/from the PCI local bus 120 when completing one element and starting the next, as the transfer proceeds without delay. The two DMA channels enable different commands to be processed concurrently with data transferred in both directions in data path 270. When a S/G list is emptied without detecting the end of the list, then the S/G list is refilled from system memory in host computer 110 using the DMA channel in command management channel 220.

Detailed Description Text (21):
Multi-tasking protocol engine 250 executes protocol commands described by a Transfer Control Block (TCB) and scatter/gather (S/G) lists to control the data transfer between the host system memory and the Fibre Channel connected device. A TCB is a data structure that contains all information for the execution of a command. TCBs are prepared by the device driver in a host system memory TCB array along with the associated S/G elements. In the illustrative computing system 100, the Fibre Channel (FC) device 160 executes high-speed Fibre Channel protocol transfers with the Multi-Tasking Protocol Engine 250 performing initialization and monitoring functions. The Multi-Tasking Protocol Engine 250 handles Fibre Channel protocol transfers by executing operations based on a clock rate referenced to a Fibre Channel clock (not shown). Multi-tasking protocol engine 250 transfers TCBs from system memory to local memory 142 of host adapter 140 for access when host computer 110 indicates the TCBs are available. Multi-tasking protocol engine 250 connects via an internal bus CIOBUS to memory port interface 230 which provides access to the local memory. Bus CIOBUS connects to multi-tasking protocol engine 250, memory port interface 230, FC data path 260, command management channel 220, and host interface 210. To access local memory, multi-tasking protocol engine 250 first acquires control of bus CIOBUS from a bus arbitrator (not shown). Multi-tasking protocol engine 250 can then read from local memory via memory port interface 230, from a buffer memory in command management channel 220, or from host interface 210. Host interface 210 or command management channel 220 can similarly

acquire control of internal bus CIOBUS and access memory via memory port interface 230.